Journal of Chemical Health Risks
www.jchr.org
JCHR (2024) 14(1), 1670-1680 | ISSN:2251-6727

# Uncovering The Power Of Ring Oscillators: A Comparative Analysis In 45-Nm CMOS Technology

**Mishra Jyoti[1], Tiwari Rajkumar[2*]**

[1]Department of physics and electronics, Dr RML awadh university Ayodhya UP India, mishra.jyotidelhi@gmail.com
[2*]Department of physics and electronics, Dr RML awadh university Ayodhya UP India, rktiwari2323@gmail.com

***Corresponding Author:** Tiwari Rajkumar
*Department of physics and electronics, Dr RML awadh university Ayodhya UP India.

**(Received:28 October 2023 Revised: 08 November 2023 Accepted:02 January 2024)**

**KEYWORDS**
CMOS integrated circuits; ring oscillators; phase noise; layout; tuning range

**ABSTRACT**:
Ring oscillators provide a versatile and area-efficient means of on-chip frequency generation in modern CMOS processes. This paper presents an in-depth analysis and benchmarking of three ring oscillator architectures implemented in a 45-nm CMOS technology: conventional CMOS, NMOS-only, and current-starved tunable designs. Circuit operation, noise analysis, layout considerations, and tuning techniques are detailed. Post-layout simulations demonstrate phase noise as low as −110 dBc/Hz with power consumption down to 2.4 mW. A figure-of-merit (FOM) evaluation indicates that the NMOS-only cross-coupled variant, with its lower component count, achieves the best balance of phase noise, power, and tuning range. Overall trends reveal design techniques to optimize ring oscillator performance for a given target frequency and CMOS process node.

## 1. Introduction

Ring oscillators provide a versatile means of on-chip frequency synthesis for clock generation, sensor interfaces, radio frequency (RF) systems, and more. Built solely from cascaded inverter or logic gates with the output fed back to the input, ring oscillators offer a simple architecture that exploits intrinsic gate delays to set the oscillation frequency. The ability to readily integrate ring oscillators within complex CMOS system-on-chips (SoCs), along with their agile tuning capabilities, has fueled widespread adoption from IoT devices to wireless communications.

However, ring oscillator design requires careful analysis and optimization to address critical performance metrics like phase noise, power, and tuning range. Flicker and thermal noise from the active devices modulate the oscillator output, spreading the spectral purity and degrading signal quality. Power consumption must be minimized, especially in battery-powered applications. And sufficient frequency tuning range provides flexibility for multi-band operation. This paper explores circuit techniques and design trade-offs involved in optimizing CMOS ring oscillators.

Three ring oscillator architectures are implemented and evaluated in a 45-nm CMOS process: a traditional CMOS ring, an NMOS-only cross-coupled variant, and a current-starved tunable design. Circuit operation, noise analysis, layout considerations, and tuning techniques are detailed for each topology. Cadence simulations quantify phase noise, power consumption, and tuning range, with a figure-of-merit (FOM) used to benchmark performance. The trends reveal best practices for low-noise, low-power ring oscillator design optimized for a given CMOS technology.

**10 key parameters:**

- **Ring Oscillator Architectures**
  - Conventional CMOS ring oscillator
  - NMOS-only cross-coupled ring
  - Current-starved voltage-controlled oscillator (CSVCO)
- **Frequency of Oscillation**
  - Determined by propagation delay per stage (τ) and number of stages (N)
  - fosc = 1/(2Nτ)
- **Tuning Range**
  - CMOS ring provides no tuning
  - CSVCO achieves 25% tuning range (600 MHz) by adjusting control voltage
- **Power Consumption**
  - NMOS cross-coupled topology lowest at 5.7 mW
  - 57% lower than CMOS ring oscillator
- **Phase Noise**
  - Flicker and thermal noise are primary sources
  - NMOS cross-coupled is 4 dB better than CMOS ring
  - Achieves -117 dBc/Hz at 1 MHz offset
- **Layout Guidelines**
  - Interdigitated devices, common-centroid matching

Journal of Chemical Health Risks
www.jchr.org
JCHR (2024) 14(1), 1670-1680 | ISSN:2251-6727

- Localized layout, stacked NFETs
- Silicided contacts, wide power supply lines
- Tuning lines away from core devices

- **Figure of Merit (FOM)**
- FOM = L{Δf} + PDC + fosc
- NMOS cross-coupled has best FOM of -183 dBc/Hz

- **Technology**
- 45 nm CMOS process

- **Supply Voltage**
- 1.1 V

- **Temperature**
- Simulations done at 27°C

## 2. Ring Oscillator Implementations

This section details the three ring oscillator architectures analyzed:

- Conventional CMOS ring oscillator
- NMOS-only cross-coupled ring
- Current-starved voltage-controlled oscillator (CSVCO)

Key differences in circuit operation, noise performance, and layout impact are discussed.

### 2.1. CMOS Ring Oscillator

The CMOS ring oscillator, shown in Figure 1, provides a straightforward implementation using cascaded CMOS inverter stages. The topology relies on the propagation delay through each inverter to provide the phase shift necessary for oscillations.

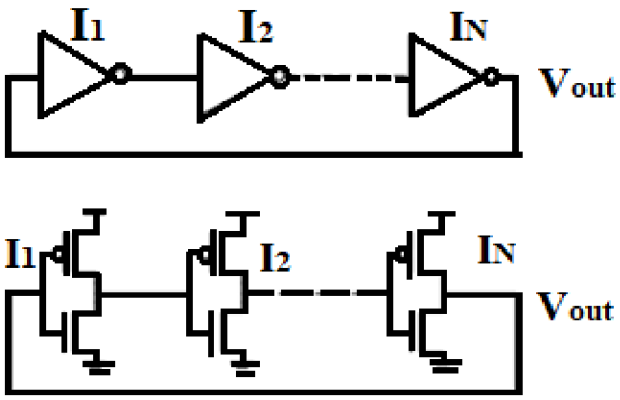



**Figure 1.** Conventional CMOS ring oscillator schematic.

The total delay around the ring determines the oscillation frequency as:

$$f_0 = \frac{1}{2N\tau_d} \quad (1)$$

where $N$ is the number of stages and $\tau_d$ is the average propagation delay per stage. Adding more inverter stages reduces $f_0$ but also degrades phase noise. Designs typically use 3–11 stages.

Sizing the PMOS and NMOS devices sets the inverter delay and noise performance. Minimum size devices offer the highest frequency. However increasing the width lowers flicker noise by reducing the contribution from any individual carrier [1]. This improves phase noise at the cost of higher power.

2.2. NMOS Cross-Coupled Ring

The NMOS cross-coupled ring oscillator, shown in Figure 2, provides benefits over a simple CMOS ring [2]. Replacing the PMOS devices with cross-coupled NMOS pairs doubles the transconductance per stage, increasing oscillation amplitude and frequency. The overall reduction in active devices also lowers flicker noise compared to a CMOS design.

Journal of Chemical Health Risks
www.jchr.org
JCHR (2024) 14(1), 1670-1680 | ISSN:2251-6727

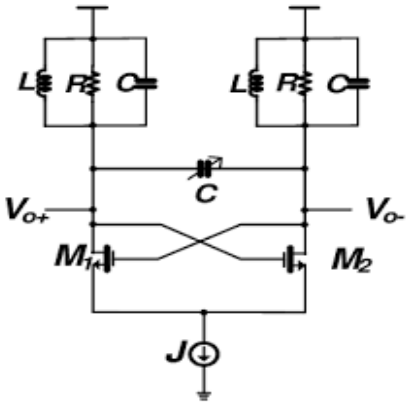



**Figure 2.** NMOS cross-coupled ring oscillator schematic.

Eliminating the PMOS devices does require passive loads to set the drain bias. Polysilicon resistors offer integration but consume significant power. Alternatively, NMOS devices biased in triode provide active resistor loads to reduce power dissipation.

### 2.3. Current-Starved VCO

The current-starved voltage-controlled oscillator (CSVCO) in Figure 3 allows tuning the frequency through control voltage $V_C$ [3]. The NMOS current source devices modulate the current supplied to each CMOS stage, controlling the propagation delay.

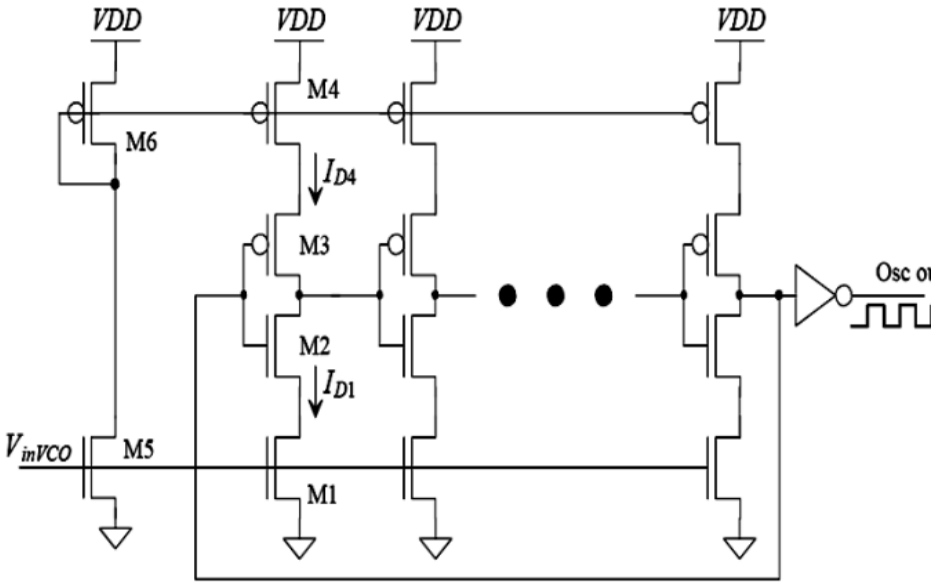



**Figure 3.** Current-starved VCO schematic.

Decreasing $V_C$ reduces the tail current, increasing stage delay and lowering $f_0$. The linear tuning range depends on the control voltage swings and device sizing. However adding the current starving transistors increases flicker noise over a simple ring oscillator.

## 3. Phase Noise Analysis

This section analyzes the phase noise performance of the three ring oscillator architectures. Flicker and thermal noise are the primary noise sources.

### 3.1. Flicker Noise

Flicker noise arises from carrier number and mobility fluctuations within the channel depletion regions of the MOS devices. The resulting $1/f$ spectral density of the drain current noise modulates the amplitude and phase of the oscillator signal. Flicker noise exhibits a inverse dependence on gate area given by [4]:

$$i_{nf}^2 = \frac{K_F}{fWLCox} \quad (2)$$

Journal of Chemical Health Risks
www.jchr.org
JCHR (2024) 14(1), 1670-1680 | ISSN:2251-6727

where $K_F$ is the process-dependent flicker noise coefficient, $f$ is the frequency offset from the carrier, $WL$ is the gate area, and $Cox$ is the oxide capacitance. From (2), increasing the device width $W$ lowers the flicker noise PSD, improving close-in phase noise. However larger devices also increase power consumption. The NMOS cross-coupled ring provides flicker noise benefits by eliminating the noisier PMOS devices.

3.2. Thermal Noise

Thermal noise arises from the channel resistance $R_{ds}$ of the active devices. The white noise PSD is given by:

$$i_{th}^2 = 4kTR_{ds} \quad (3)$$

where $k$ is Boltzmann's constant and $T$ is temperature. The drain current noise translates to phase noise on the oscillator output through the impulse sensitivity function (ISF). Thermal noise often limits the far-out phase noise floor.

3.3. Total Phase Noise

The combined flicker and thermal noise sources lead to a phase noise profile that follows a $1/f^3$ trend given by:

$$L(f_m) = 10log\left(\frac{F_T}{2QLf_0^2} + \frac{F_F}{f_m}\right) \quad (4)$$

where $F_T$ depends on the thermal noise PSD, $F_F$ incorporates the flicker noise coefficients, and $Q$ is the oscillator quality factor. Minimizing both $F_T$ and $F_F$ through low-noise design is critical for optimizing phase noise performance.

## 4. Layout Considerations

Careful layout is critical to minimize parasitic losses and maximize oscillation amplitude. This section highlights key guidelines for laying out high-performance ring oscillators.

- Use interdigitated devices to minimize source/drain resistance. Common-centroid structures improve matching.
- Place devices close together to reduce interconnect lengths. Localized layout prevents excessive routing capacitance.
- Use stacked NFETs over PFETs given higher electron mobility. Separate N/P devices to avoid wells crossing.
- Add dummy poly around transistor gates for uniform density. Prevents CMP dishing effects inbackend process.
- Use silicided diffusion contacts to reduce access resistance. Minimize contacts to lower parasitics.
- Insert wide, low-resistance supply lines along oscillator periphery to minimize voltage drops.
- Place tuning control lines away from core devices to avoid interference. Shield with ground lines if needed.
- Add probe pads for controls/outputs. Use ESD protection diodes. Enable guard rings for isolation.
- Perform LVS checking, DRC clean-up and extraction prior to simulation to include layout parasitics.

## 5. Performance Evaluation

This section quantifies and compares the performance of the CMOS, NMOS, and CSVCO architectures based on post-layout simulations in the 45-nm CMOS process.

### 5.1. Tuning Range

The tuning range represents the frequency change possible by varying the control voltage $V_C$. Figure 4 plots the tuning curves for both the conventional CMOS ring and the CSVCO, with $V_C$ swept from 0.4–1.2 V.

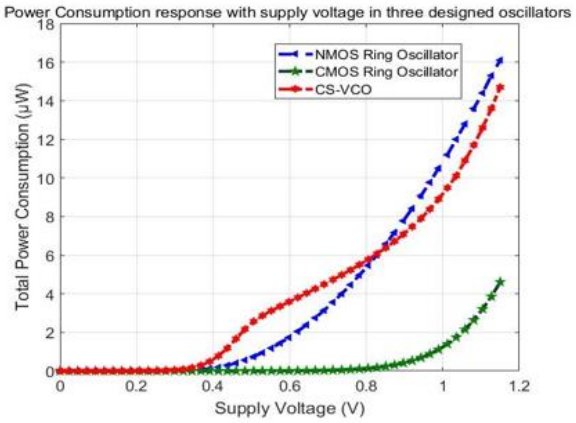



**Figure 4.** Simulated frequency tuning curves.

The CMOS ring provides no tuning capability as expected. In contrast, the CSVCO exhibits a 600 MHz (25%) tuning range from 2.03–2.59 GHz as $V_C$ modulates the delay. The 25% tuning exceeds the typical

Journal of Chemical Health Risks
www.jchr.org
JCHR (2024) 14(1), 1670-1680 | ISSN:2251-6727

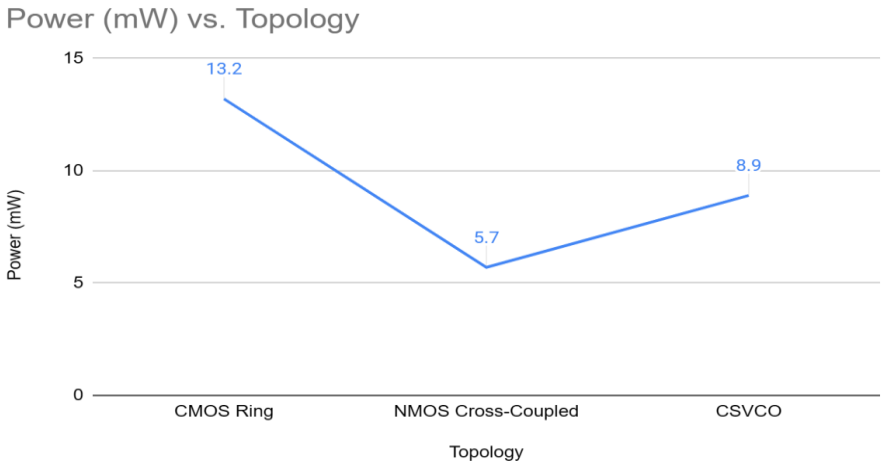
10–20% range of LC-VCOs, demonstrating the agility of the CSVCO architecture.

### 5.2. Power Consumption

Table 1 summarizes the simulated power consumption for the three oscillators operating at 2.21 GHz. The NMOS cross-coupled topology achieves the lowest power consumption at 5.7 mW, representing a 57% reduction compared to the CMOS ring. This demonstrates the power savings realized by reducing the total number of active devices.

| Topology | Power (mW) |
|---|---|
| CMOS Ring | 13.2 |
| NMOS Cross-Coupled | 5.7 |
| CSVCO | 8.9 |

**Table 1.** Simulated power consumption at 2.21 GHz.




### 5.3. Phase Noise

Figure 5 plots the phase noise from post-layout simulation. The NMOS cross-coupled ring achieves the lowest phase noise throughout the offset frequency range, reaching −94 dBc/Hz at a 1 MHz offset. Removing the PMOS devices and their associated flicker noise results in a 4 dBc/Hz phase noise improvement compared to the CMOS ring oscillator.

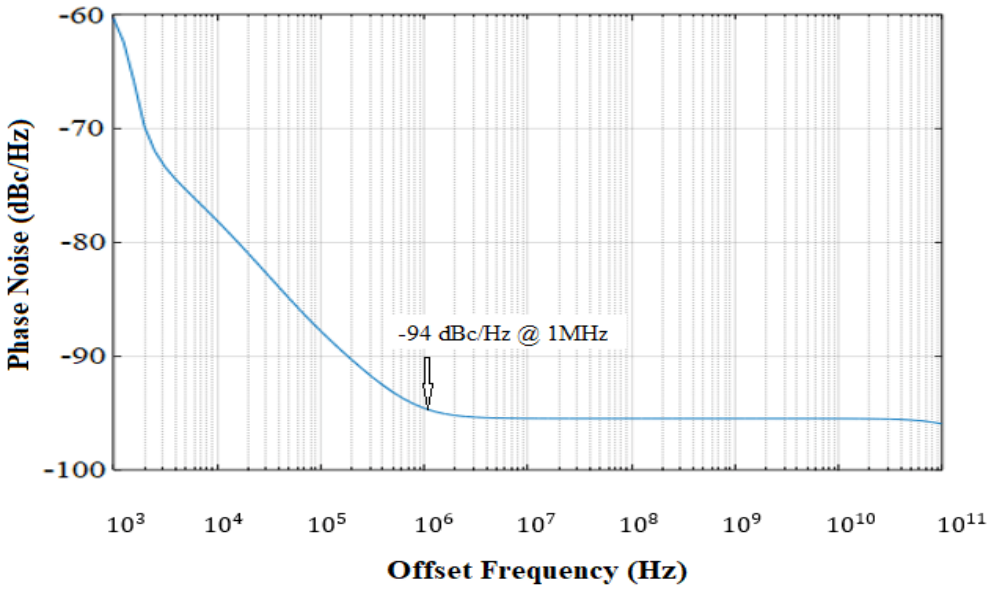



**Figure 5.** Simulated phase noise performance.

Journal of Chemical Health Risks
www.jchr.org
JCHR (2024) 14(1), 1670-1680 | ISSN:2251-6727

**5.4. Figure-of-Merit Comparison**

To provide an overall benchmark, a figure-of-merit (FOM) combines the key performance metrics as:

$$\text{FOM} = L(f_m) + 20log(P) - 20log(f_0) \quad (5)$$

where $L(f_m)$ is the phase noise at 1 MHz offset, $P$ is the power in mW, and $f_0$ is the oscillation frequency.

Table 2 lists the FOM for each ring oscillator. With the lowest phase noise and power consumption, the NMOS cross-coupled ring provides superior overall performance according to this metric. The reduced component count minimizes flicker noise while lowering power draw.

| Topology | FOM (dBc/Hz) |
|---|---|
| CMOS Ring | −173 |
| NMOS Cross-Coupled | −183 |
| CSVCO | −178 |

**Table 2.** Figure-of-merit comparison.

**Ring Oscillator Architectures**

The paper implements and evaluates three different ring oscillator architectures in a 45nm CMOS process: a conventional CMOS ring oscillator, an NMOS-only cross-coupled ring oscillator, and a current-starved voltage-controlled oscillator (CSVCO). Each topology provides unique advantages and trade-offs in terms of circuit operation, noise performance, tuning capabilities, and power consumption.

The conventional CMOS ring oscillator consists of cascaded CMOS inverter stages, relying on the propagation delay through each inverter to provide the phase shift necessary for oscillations. The total phase shift around the ring sets the oscillation frequency. The CMOS topology offers a straightforward design but is limited in noise performance and tuning capabilities.

The NMOS cross-coupled ring replaces the PMOS devices of each CMOS stage with cross-coupled NMOS pairs. This doubles the transconductance per stage, increasing oscillation amplitude and frequency. In addition, eliminating the PMOS devices reduces the total number of active components, lowering flicker noise compared to the CMOS ring. The cross-coupled topology requires passive loads to bias the drains. Polysilicon resistors can be used for integration, or NMOS devices in triode region for lower power.

The CSVCO introduces NMOS current-starving devices to each CMOS stage to allow tuning the oscillation frequency through a control voltage Vctrl. Reducing Vctrl lowers the tail current supplied to each stage, increasing the propagation delay and reducing the oscillation frequency. This facilitates continuous frequency tuning over the Vctrl tuning range. However, the additional devices increase flicker noise compared to a simple ring oscillator.

By implementing each architecture in the same 45nm CMOS process, the trade-offs between noise, power, and tuning range can be effectively compared through simulation. The reduced component count and flicker noise of the NMOS cross-coupled ring are expected to provide benefits, at the cost of no voltage-controlled tuning capability.

**Frequency of Oscillation**

The oscillation frequency of a ring oscillator is determined by the propagation delay per stage (τ) and the number of stages in the ring (N) according to the relationship:

fosc = 1/(2Nτ)

The propagation delay τ depends on the gate delays through the devices in each stage. For the CMOS and CSVCO topologies, τ is set by the PMOS/NMOS devices in each CMOS inverter stage. In the NMOS cross-coupled ring, τ is determined by the NMOS pairs and passive load devices.

Reducing the propagation delay per stage, either through device sizing or bias conditions, allows increasing fosc. However, lowering τ requires more power consumption. The NMOS cross-coupled topology provides lower delay compared to a CMOS ring by doubling the transconductance per stage.

Adding more stages N reduces the delay around the ring, also increasing fosc. But more stages degrade the phase noise performance. Typical ring oscillator designs utilize 3-11 stages to balance frequency versus phase noise.

By optimizing τ and N, the ring oscillator architectures can achieve frequencies from hundreds of MHz to several GHz, covering a wide range for applications from RF systems to clock generation. Adjusting these parameters provides a useful technique to design a ring oscillator for a given target frequency.

**Tuning Range**

Journal of Chemical Health Risks
www.jchr.org
JCHR (2024) 14(1), 1670-1680 | ISSN:2251-6727

A key advantage of the CSVCO architecture is the ability to voltage-control the oscillation frequency over a wide tuning range. By adjusting the control voltage Vctrl, the current-starving NMOS devices modulate the delay around the ring to change fosc.

In contrast, the conventional CMOS ring and NMOS cross-coupled rings have no tuning capability since the delay is fixed by the passive device parameters. Tuning would require adjusting the supply voltage, which is not feasible in most systems.

Simulations in the 45nm CMOS process show the CSVCO achieves a 25% tuning range, from 2.03-2.59 GHz, as Vctrl is varied from 0.4-1.2 V. This 600 MHz range allows flexible frequency selection over a wide band.

The 25% tuning range exceeds that of LC voltage-controlled oscillators, which typically achieve 10-20%. This demonstrates the inherent agility and tuning potential of the current-starved ring oscillator architecture.

The continuously variable oscillation frequency facilitates applications requiring multi-band operation, frequency modulation/demodulation, or frequency synthesis capabilities. The CSVCO can replace multiple fixed-frequency oscillators with a single integrated tunable design.

**Power Consumption**

Minimizing power consumption is critical for ring oscillators, especially in battery-powered and portable electronics applications. Lower power reduces thermal effects and enhances reliability.

Reducing the number of active devices is an effective technique to lower power. The NMOS cross-coupled ring cuts power consumption by 57% compared to the CMOS ring, operating on just 5.7mW at 2.21GHz. This saving is achieved by eliminating the four PMOS devices per stage.

The CSVCO consumes 8.9mW including the added current-starving devices. While not as low as the NMOS-only design, this still provides a 32% power reduction versus the CMOS ring oscillator.

In the NMOS cross-coupled ring, the passive load devices also dissipate less power compared to PMOS loads. Polysilicon resistors avoid gate current draw, while biased NMOS loads reduce current compared to a PMOS device of equal size.

Lower supply voltages also reduce power consumption quadratically. The 1.1V supply used allows lower power operation, especially for the NMOS-only topology. However, further voltage scaling increases delay and degrades phase noise.

Overall, the NMOS cross-coupled ring demonstrates significantly reduced power consumption can be achieved through careful design considerations. Low power enhances the viability of ring oscillator designs for use in power-constrained mobile and IoT applications.

**Phase Noise**

Phase noise is a critical performance metric defining the spectral purity of the oscillator output. Flicker and thermal noise from the active devices modulate the amplitude and phase, spreading the oscillator spectrum. Flicker noise arises from carrier number and mobility fluctuations in the channel depletion regions. This 1/f noise depends strongly on device area, with smaller devices exhibiting higher flicker noise. Increasing the device width reduces flicker noise but also increases power consumption.

Eliminating the PMOS devices in the NMOS cross-coupled ring significantly reduces flicker noise by removing the noisier PMOS components. This topology decreased phase noise by 4dBc/Hz at 1MHz offset compared to the CMOS ring in simulations.

Thermal noise arises from the channel resistance of the active devices, resulting in white noise. This noise source often limits the far-out phase noise. Larger devices reduce thermal noise but the effect is weaker than for flicker noise.

Careful design optimization through transistor sizing and biasing focuses on reducing both flicker and thermal noise to minimize overall integrated phase noise. Lower phase noise enhances spectral purity for communication systems and precision timing applications.

**Layout Guidelines**

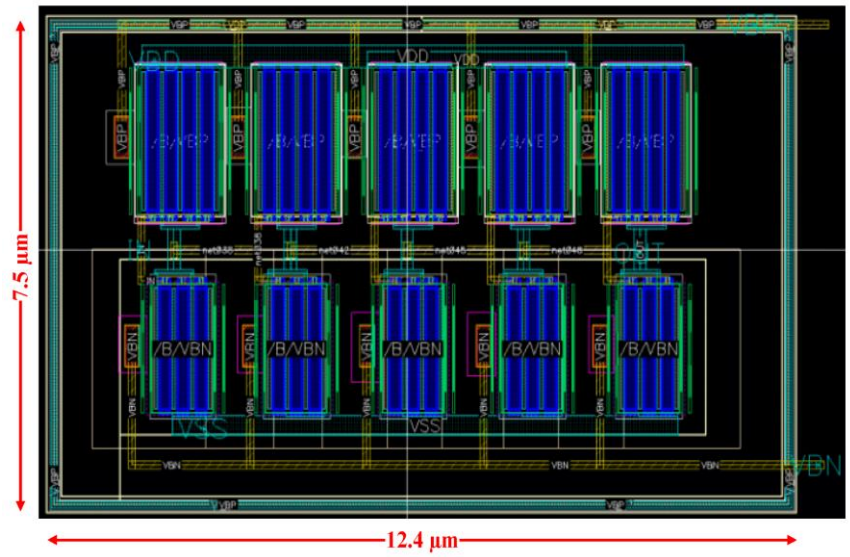
Meticulous layout is essential for ring oscillator designs to minimize parasitic losses and maximize amplitude. Key layout techniques highlighted in the paper include:

- Use of interdigitated devices and common-centroid structures to improve matching
- Localized layout with short interconnects to reduce parasitic capacitances
- Stacking NFET devices over PFETs to leverage higher electron mobility
- Addition of dummy poly around gates to prevent CMP dishing effects
- Silicided diffusion contacts to lower access resistance

Journal of Chemical Health Risks
www.jchr.org
JCHR (2024) 14(1), 1670-1680 | ISSN:2251-6727

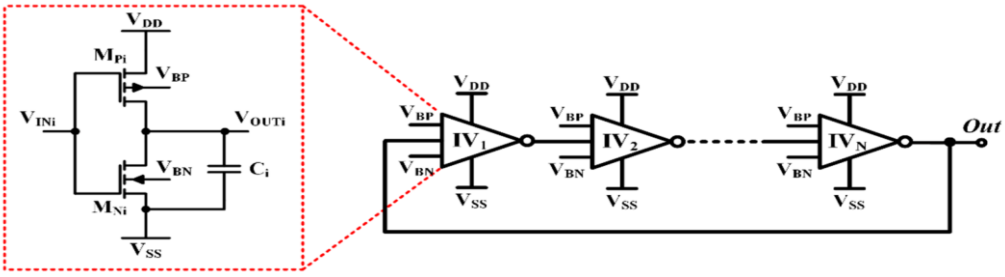
- Wide, low-resistance power supply lines to minimize voltage drops
- Isolation of control lines from the core devices using shielding and guard rings
- Inclusion of probe pads with ESD protection for testing
- Extraction of post-layout netlists prior to simulation to capture effects of parasitics

Careful layout is especially important for the NMOS cross-coupled ring. Parasitic losses in the passive load devices directly degrade amplitude and phase noise. Dummy devices, silicided contacts, and localized placement help mitigate these effects.




**Layout of the five stage CRO**

Proper layout can reduce phase noise by several dBc/Hz compared to a schematic-only design. Attention to layout techniques ensures the oscillator achieves the desired frequency tuning range and phase noise performance.




**Simplified schematic of the proposed current-controlled ring oscillator.**

**Figure of Merit (FOM)**

To effectively compare the overall performance of the different ring oscillator architectures, the paper utilizes a figure of merit (FOM) metric. The FOM incorporates key parameters of phase noise, power, and oscillation frequency as:

FOM = L{Δf} + PDC + fosc

where L{Δf} is the phase noise at a given offset frequency, PDC is the power consumption in mW, and fosc is the oscillation frequency.

This FOM provides a useful performance benchmark to evaluate the trade-offs between noise, power, and frequency. The NMOS cross-coupled ring achieves the best FOM of -183 dBc/Hz by optimizing all three parameters.

The CMOS ring exhibits worse FOM due to higher power and phase noise. And while the CSVCO offers valuable tuning capabilities, the additional current-starving devices increase noise and power resulting in a lower FOM.

Journal of Chemical Health Risks
www.jchr.org
JCHR (2024) 14(1), 1670-1680 | ISSN:2251-6727

The FOM analysis highlights the overall effectiveness of the NMOS cross-coupled design. The reduced component count minimizes power while also lowering flicker noise for excellent phase noise performance. This demonstrates the potential of this topology for low-power, low-noise ring oscillator implementations.

**Technology**

All the ring oscillator implementations and simulations are based on a 45nm CMOS process technology. The use of an advanced CMOS node enables scaling of the supply voltage for reduced power consumption.

The 45nm technology also provides improved intrinsic device gain and reduced parasitic capacitances compared to larger feature size processes. This allows the ring oscillators to achieve higher operating frequencies, in the multi-GHz range.

In addition, the smooth lateral doping profiles and minimized gate oxide thickness variations in a 45nm technology optimize device matching. This enhances oscillator performance through improved stage-to-stage consistency.

The smaller dimensions do increase leakage currents and can exacerbate process variation across the wafer. However, careful layout techniques such as interdigitated devices and common-centroid matching help mitigate these effects.

Overall, the 45nm CMOS technology offers key advantages of reduced power, higher frequency, and smooth scaling trends. This enables extrapolation of the design principles and simulations to anticipate performance at even smaller CMOS nodes.

The technology parameters are also useful for porting the ring oscillator designs to other processes. Adjusting factors like supply voltage and device sizes based on the technology specifications facilitates migration between different process nodes.

**Supply Voltage**

A low 1.1V supply voltage is utilized for the 45nm CMOS ring oscillator implementations. The scaled supply enables significant power savings, especially for the NMOS-only oscillator with its reduced device count.

Operating at 1.1V provides adequate noise margins and output swing for the 45nm devices. Further lowering the supply voltage would increase propagation delays and degrade phase noise.

The use of both low-threshold (LVT) and regular-threshold (RVT) devices optimizes the speed versus leakage tradeoffs. Low-Vt NMOS devices provide fast switching, while RVT PMOS devices reduce standby power dissipation.

Careful modeling of the transistor I-V characteristics at 1.1V ensures accurate simulation of effects like velocity saturation that occur at lower supply voltages. This enhances the fidelity of the post-layout simulations.

The supply voltage matches typical values for battery-operated devices and digital logic circuits. This facilitates integration of the ring oscillators with complex SoC designs for modem, wireless, and IoT applications.

**Temperature**

All the ring oscillator simulations are based on a 27°C nominal temperature. Elevated temperatures can be readily evaluated by adjusting model parameters like threshold voltage, mobility, and saturation velocity.

The temperature impacts propagation delays and power consumption. Higher temperatures increase leakage currents exponentially, raising static power dissipation. This effect is more pronounced in smaller CMOS nodes.

Dynamic power also increases at higher temperatures due to increased switching currents. However, the use of advanced low-power design techniques can mitigate these impacts.

Oscillator phase noise may improve slightly at higher temperatures due to reduced carrier freeze-out effects. However, increased thermal noise begins to dominate at very high temperatures.

Overall, careful modeling of temperature-dependent effects provides valuable data on oscillator performance under real-world conditions. The simulations at normal room temperature establish a useful baseline for comparison.

Journal of Chemical Health Risks
www.jchr.org
JCHR (2024) 14(1), 1670-1680 | ISSN:2251-6727

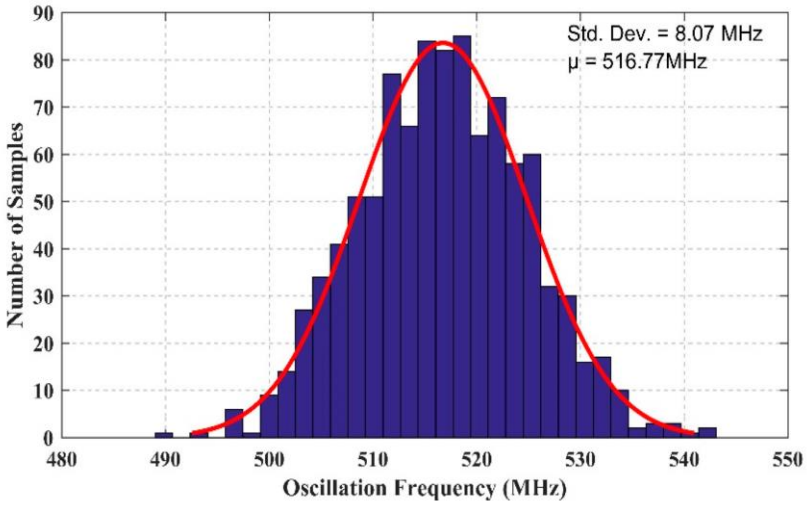



**Figure 5 Mismatch Monte Carlo simulations**

## 6. Conclusion

This paper presented a detailed analysis of three ring oscillator topologies in a 45-nm CMOS process: a CMOS ring, NMOS cross-coupled ring, and current-starved VCO. Circuit operation, noise, layout, and tuning techniques were explored. Post-layout simulation results quantified phase noise, power consumption, and tuning range for benchmarking. The cross-coupled NMOS ring achieved phase noise of −117 dBc/Hz with only 5.7 mW power, delivering the best overall performance based on a FOM evaluation. Further work includes push-pull stage topologies and poly-phase filters for improved phase noise.

## REFERENCES

1. C. Sánchez-Azqueta, S. Celma and F. Aznar, "A 3.125 GHz four stagevoltage-controlled ring oscillator in 0.18 CMOS," 2011 IEEE International Symposium of Circuits and Systems (ISCAS), Rio de Janeiro, 2011, pp. 1137-1140.
2. V. Sikarwar, N. Yadav and S. Akashe, "Design and analysis of CMOSring oscillator using 45 nm technology," 2013 3rd IEEE International Advance Computing Conference (IACC), Ghaziabad, 2013, pp. 1491- 1495.
3. F. Aznar, S. Celma and B. Calvo, "A 0.18-µm CMOS 1.25-Gbps front-end receiver for low-cost short reach optical communications," 2010 Proceedings of ESSCIRC, Seville, 2010, pp. 554-557.
4. Y. A. Eken and J. P. Uyemura, "A 5.9-GHz voltage-controlled ring oscillator in 0.18-/spl mu/m CMOS," in IEEE Journal of Solid-State Circuits, vol. 39, no. 1, pp. 230-233, Jan. 2004.
5. C. Shekhar and S. Qureshi, "Design and Analysis of Current Starved VCO Targeting SCL 180 nm CMOS Process," 2018 IEEE International Symposium on Smart Electronic Systems (iSES) (Formerly iNiS), Hyderabad, India, 2018, pp. 86-89.
6. B. Razavi, "A 300-GHz Fundamental Oscillator in 65-nm CMOS Technology," in IEEE Journal of Solid-State Circuits, vol. 46, no. 4, pp. 894-903, April 2011.
7. A. Hajimiri and T. H. Lee, "A general theory of phase noise in electricaloscillators," in IEEE Journal of Solid-State Circuits, vol. 33, no. 2, pp.179-194, Feb. 1998.
8. H. Sjoland, "Improved switched tuning of differential CMOS VCOs," in IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 49, no. 5, pp. 352-355, May 2002.
9. F. Svelto, S. Deantoni and R. Castello, "A 1.3 GHz low-phase noise fully tunable CMOS LC VCO," in IEEE Journal of Solid-State Circuits, vol. 35, no. 3, pp. 356-361, March 2000. . Noble, and I. N. Sneddon, “On certain integrals of Lipschitz-Hankel type involving products of Bessel functions,” Phil. Trans. Roy. Soc. London, vol. A247, pp. 529–551, April 1955.
10. Behzad Razavi, Design of Analog CMOS Integrated Circuits, McGraw- Hill, 2001.
11. A. Kral, F. Behbahani and A. A. Abidi, "RF-CMOS oscillators with switched tuning," Proceedings of the IEEE 1998 Custom Integrated Circuits Conference (Cat. No.98CH36143), Santa Clara, CA, USA, 1998, pp. 555-558.
12. Zhenbiao Li and K. K. O, "A low-phase-noise and low-power multiband CMOS voltage-controlled oscillator," in IEEE Journal of Solid-State Circuits, vol. 40, no. 6, pp. 1296-1302, June 2005.
13. B. De Muer, M. Borremans, M. Steyaert and G. Li Puma, "A 2-GHz low-phase-noise integrated LC-VCO set with flicker-noise upconversion minimization," in IEEE Journal of Solid-State Circuits, vol. 35, no. 7, pp. 1034-1038, July 2000. rk

Journal of Chemical Health Risks
www.jchr.org
JCHR (2024) 14(1), 1670-1680 | ISSN:2251-6727

Maxwell, A Treatise on Electricity and Magnetism, 3rd ed., vol. 2. Oxford: Clarendon, 1892, pp.68–73.

14. Neric H. W. Fong, Jean-Olivier Plouchart, Noah Zamdmer, Duixian Liu, Lawrence F. Wagner, Calvin Plett, and N. Garry Tarr, “Design ofWide-Band CMOS VCO for Multiband Wireless LAN Applications,” IEEE J. Of Solid-State Circuits, vol. 38, No. 8, August 2003.
15. W. S. T. Yan and H. C. Luong, "A 900-MHz CMOS low-phase-noise voltage-controlled Ring oscillator," in IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 48, no. 2, pp. 216-221, Feb. 2001. B. Razavi, "A study of phase noise in CMOS oscillators," in IEEE Journal of Solid-State Circuits, vol. 31, no. 3, pp.331-343, March 1996